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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 09/501,074 | 02/09/2000 | Michael Pothier | Ntl-3.2.3078/2134 Pothier | 3367 |

35437 7590 11/17/2004

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| EXAMINER | |
|---|---|
| SHAH, CHIRAG G | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2664 | |

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) |
|---|---|---|
| | 09/501,074 | POTHIER ET AL. |
| | Examiner | Art Unit |
| | Chirag G Shah | 2664 |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *8/6/04* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6-12,14-20,22-28,30-36 and 38-40* is/are rejected.

7)☒ Claim(s) *5, 13, 21, 29, and 37* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

## DETAILED ACTION

### *Claim Rejections - 35 USC § 102*

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-3, 8-11, 16-19, 24-27, 32-35 and 40 rejected under 35 U.S.C. 102(e) as being anticipated by Lauret (U.S. Patent No. 6,252,850).

Referring to claim 1, 9, 17, 25, and 33, Lauret discloses in column 2, lines 40-64 of an apparatus for synchronizing a clock (adaptive clock recovery mechanism) with data received via asynchronous transfer mode (ATM receiver) comprising: a plurality of buffers (first and second buffers as disclosed in column 2, lines 41-54) connected to the ATM (ATM network) and circuitry configured for reading out data from the buffers at a clock rate specified by the clock (a selectable clock source can comprise a selector having at least first and second clock inputs for respective clock frequencies or rates, a clock output for outputting a clock frequency/rate for controlling the reading of cells from the first buffer and a first buffer fill level input, the selector being arranged to determine a fill level of the buffer as disclosed in column 3, lines 20-30) and a regulating circuit (first buffer fill level controller as disclosed in column 2, line 65) configured to regulate the clock rate according to transmission rate data ( the first buffer fill level controller (regulating circuit) that comprises a selectable clock sources for supplying a selectable one of at

least a first and a second clock frequency for outputting cells from the first buffer, the selectable clock source being responsive to a fill level of the first buffer to a select a clock frequency and thus, providing a simple control structure for keeping the rate of output of cells form the first buffer within a predetermined range as disclosed in column 2, lines 40 to column 3, lines 3 and claims 1 and 2 as claim.

Referring to claim 2, 10, 18, 26, and 34, Lauret discloses in column 2, lines 40-58, column 3, lines 20-60 and in column 4, lines 3-59 the apparatus wherein, the regulating circuit (first buffer fill level controller) regulates the clock rate (selectable clock frequency) so that the data is read out from the buffers at a rate substantially equal to a rate at which the data is transmitted via the asynchronous transmission medium (The first buffer controls the range of cell rates supplied to the second buffer, once locked, the phase locked loop can provide a stable output frequency locked substantially to the service clock frequency. In other words, a second buffer having an input connected to receive cells from the output of the first buffer and an output; and a second buffer fill level controller connected to the second buffer to cause a rate of cell output from the second buffer to be locked substantially to the service clock frequency) as claim.

Referring to claim 3, 11, 19, 27, and 35, Lauret discloses in column 4, lines 3-59 the apparatus wherein, the data is input to the transmission medium at a predetermined constant rate (A rate of output of the second buffer is locked substantially to the frequency of the predetermined service clock of the CBR source (input) application); and the clock rate is initially set to the predetermined constant rate (The adaptive clock recovery mechanism enable the clock

of a CBR service to be recovered at an ATM receiver where the service is being emulated from an ATM transmitter as disclosed in column 2, lines 40-58) as claim.

Referring to claim 8, 16, 24, 32, and 40, Lauret discloses in column 1, lines 6-40 and column 2, lines 40-58 wherein the data is organized into packets (or cells) and the data was synchronous data (voice, data and video with CBR) prior to transmission via the asynchronous (Asynchronous Transfer Mode), and wherein the regulating circuit (first buffer fill level controller disclosed in column 3, lines 65 to column 4, lines 30) regulates the clock (through the use of the selectable clock source having first and second clock frequencies dependent on the fill level as disclosed in column 4, lines 4-30) according to a rate of change of transmission delay occurring in the transmission medium (the selectable clock source being responsive to a fill level of the buffer to select a clock frequency, thus selectable clock source selects the first clock frequency when a fill level of the first buffer is greater than a threshold value and selects the second clock when a fill level of the buffer is less than the threshold value) as claim.

### *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 6, 7, 14, 15, 22, 23, 30, 31, 38 and 39 rejected under 35 U.S.C. 103(a) as being unpatentable over Lauret in view of Owada (U.S. Patent No. 6,219,396).

Referring to claim 6, 14, 22, 30, and 38, Lauret discloses in column 1, lines 6-40 and column 2, lines 40-58 wherein the data is organized into packets (or cells) and the data was synchronous data (voice, data and video with CBR) prior to transmission via the asynchronous (Asynchronous Transfer Mode), and wherein the regulating circuit (first buffer fill level controller disclosed in column 3, lines 65 to column 4, lines 30) regulates the clock (through the use of the selectable clock source having first and second clock frequencies dependent on the fill level as disclosed in column 4, lines 4-30) according to a rate of change of transmission delay occurring in the transmission medium (the selectable clock source being responsive to a fill level of the buffer to select a clock frequency, thus selectable clock source selects the first clock frequency when a fill level of the first buffer is greater than a threshold value and selects the second clock when a fill level of the buffer is less than the threshold value). Lauret fails to disclose the regulating circuit regulates the clock according to a ratio of a number of packets received during a predetermined period and a number of packets synchronously transmitted during the predetermined period. Owada discloses in column 3,lines lines 6-65 and column 4, lines 44 to column 5, lines 59 that regulating circuit regulates the packets received during a predetermined interval and the number of data packets synchronously transmitted during a predetermined interval by means of a monitoring circuit. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Lauret to include the teaching of Owada in order to achieve regulation and regeneration that would enable the clock rate to be synchronized with the transmission data rate efficiently (without delay ensuring no data loss).

Referring to claim 7, 15, 23, 31, and 39, Lauret discloses in column 1, lines 6-40 and column 2, lines 40-58 wherein the data is organized into packets (or cells) and the data was

synchronous data (voice, data and video with CBR) prior to transmission via the asynchronous (Asynchronous Transfer Mode), and wherein the regulating circuit (first buffer fill level controller disclosed in column 3, lines 65 to column 4, lines 30) regulates the clock (through the use of the selectable clock source having first and second clock frequencies dependent on the fill level as disclosed in column 4, lines 4-30) according to a rate of change of transmission delay occurring in the transmission medium (the selectable clock source being responsive to a fill level of the buffer to select a clock frequency, thus selectable clock source selects the first clock frequency when a fill level of the first buffer is greater than a threshold value and selects the second clock when a fill level of the buffer is less than the threshold value). Lauret fails to disclose of regulating circuit regulates said clock according to a ratio of a time between two successively received packets and a time between synchronous transmission of two successive packets. Owada discloses in claim 5, and column 3,lines lines 6-65 and column 4, lines 44 to column 5, lines 59 of regulating at least two read clock signals that differ in rate from each other that have successively received packets. The program clock acquisition circuit extracts the timing signals from the read transmitted data RD and restores the program clock signal. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Lauret to include the teaching of Owada in order to achieve regulation and regeneration that would enable the clock rate to be synchronized with the transmission data rate efficiently (without delay ensuring no data loss).

5. Claims 4, 12, 20, 28 and 36 rejected under 35 U.S.C. 103(a) as being unpatentable over Lauret in view of Hartmann et al. (U.S. Patent No. 6,047,002).

Referring to claim 4, 12, 20, 28, and 36, Lauret discloses in column 2, lines 40-64 of an apparatus for synchronizing a clock (adaptive clock recovery mechanism) with data received via asynchronous transfer mode (ATM receiver) comprising: a plurality of buffers (first and second buffers as disclosed in column 2, lines 41-54) connected to the ATM (ATM network) and circuitry configured for reading out data from the buffers at a clock rate specified by the clock (a selectable clock source can comprise a selector having at least first and second clock inputs for respective clock frequencies or rates, a clock output for outputting a clock frequency/rate for controlling the reading of cells from the first buffer and a first buffer fill level input, the selector being arranged to determine a fill level of the buffer as disclosed in column 3, lines 20-30) and a regulating circuit (first buffer fill level controller as disclosed in column 2, line 65) configured to regulate the clock rate according to transmission rate data ( the first buffer fill level controller (regulating circuit) that comprises a selectable clock sources for supplying a selectable one of at least a first and a second clock frequency for outputting cells from the first buffer, the selectable clock source being responsive to a fill level of the first buffer to a select a clock frequency and thus, providing a simple control structure for keeping the rate of output of cells form the first buffer within a predetermined range as disclosed in column 2, lines 40 to column 3, lines 3 and in column 4, lines and claims 1 and 2. Lauret fails to disclose buffers are circularly arranged. Hartmann discloses in the abstract, figure 5 and in column 2 lines 30 to column 3, lines 67 that communication also includes buffers coupled to each of the port adapters for buffering data (asynchronous ATM) between port adapter and communication traffic circle. Therefore, it would have been obvious to one of ordinary skill in the art to modify the teachings of Lauret to

include the teachings of Hartmann in order to provide improved synchronous packets transmission.

### *Allowable Subject Matter*

6. Claims 5, 13, 21, 29, and 37 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Response to Arguments*

7. Applicant's arguments filed 8/6/04 have been fully considered but they are not persuasive.

Referring to claims 1, 9, 17, 25 and 33, Applicant argues that Laurent does not set out an element of regulating circuit/means for regulating the clock rate according to the transmission rate of the data. Examiner respectfully disagrees and redirects Applicant to Laurent reference, specifically in column 2, lines 40 to col. 3, lines 16 and in claims 1 & 2, of buffer fill level controller that functions as a regulating circuit that comprises a selectable/regulating clock source according to the transmission rate of the data (received in the fill level of the buffer). The selectable clock source is responsive to a fill level (rate of fill level) of the first buffer to select/regulate the clock frequency accordingly. Thus, the use of regulating clock rate dependent on the fill level (rate of fill level) of the buffer provides a simple control structure for keeping the rate of the output of cells from the buffer within a predetermined level. Thus, claims 1, 9, 17, 25, 33 are anticipated since the all the limitations of the respective claims are disclosed in Laurent reference.

Referring to claims 6, 7, 14, 15, 22, 23, 30, 31 and 38, Applicant argues that Laurent fails to contain a suggestion or motivation to combine the teachings of Owada to achieve Applicant's claimed invention. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to one of ordinary skill in the art to modify the teachings of Lauret to include the teaching of Owada in order to achieve regulation and regeneration that would enable the clock rate to be synchronized with the transmission delay rate efficiently (without delay ensuring no data loss). Therefore, claims 6, 7, 14, 15, 22, 23, 30, 31 and 38 stand rejected.

Referring to claim 4, 12, 20, 28 and 36, Applicant argues that there is no teaching or suggestion to combine the two references. Applicant respectfully disagrees because the limitation includes all the listed limitation except for the buffers being circularly arranged. The motivation with the respective claims is provided for the reasons of arranging the buffers circularly as opposed to arranging the buffers conventionally. Thus, the motivation, although Hartmann and Laurent may deal with very different subject matter is proper due to the limitation of buffers being circularly arranged that the primary reference fail to disclose. Therefore, claims 4, 12, 20, 28 and 36 remain rejected.

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

**Any response to this final action should be mailed to:**

**Box AF**
Commissioner of Patents and Trademarks
Washington, D.C. 20231

**Or faxed to:**

(703)305-9051, (for formal communications; please mark "EXPEDITED PROCEDURE)

**Or:**

(703)305-5403 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2021 Crystal Drive, Arlington, VA., Sixth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chirag G Shah whose telephone number is 571-272-3144. The examiner can normally be reached on M-F 8:00 to 4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wellington Chin can be reached on 571-272-3134. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

cgs
October 25, 2004

Ajit Patel
Primary Examiner